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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/668,166	09/24/2003	Toshio Kimura	1035-473	4031

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EXAMINER	
ARENA, ANDREW OWENS	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 10/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/668,166	KIMURA ET AL.	
	Examiner	Art Unit	
	Andrew O. Arena	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4,5,7-9,11-13,15-17,19 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 2, 4, 5, 7, 8, 9, 11, 12, 13, 15, 16, 17, 19 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1, 2, 4, 5, 7, 8, 9, 11, 12, 13, 15, 16, 17, 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anderson (US 6,661,100) in view of Hayasaka (US 6,809,421).

Re claim 1, Anderson discloses (Fig 2) a semiconductor device, comprising:

a plurality of spaced apart electrodes (connections 205; col 4 ln 2) with equal cross-sectional areas on a semiconductor chip (200; col 3 ln 65), wherein

at least two of the plurality of electrodes are connected to one another to form a first high-current electrode (210) that is in communication with a power supply (VDD; col 4 ln 10-12),

at least another two of the plurality of electrodes are connected to one another to form a second high-current electrode (220) that is in communication with ground (GND; col 4 ln 4-6),

a particular signal-routing electrode (205) is formed of only one of the plurality of through electrodes.

Anderson differs from the claimed invention in not disclosing through electrodes and in not disclosing a non-contact through electrode.

Hayasaka discloses (Fig 4) through electrodes (4; col 10 ln 30-34) which electrically link a front surface of the chip to a back surface of the chip.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Anderson in view of Hayasaka by forming at least the peripheral electrodes (205, 212, 220) to be through electrodes which electrically link a front surface of the chip to a back surface of the chip; at least to allow stacking and connecting more than two chips (Hayasaka: col 10 ln 46-54).

Hayasaka discloses non-contact through electrodes used only for heat radiation (col 11 ln 15-16).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to further modify Anderson in view of Hayasaka such that at least one of the plurality of through electrodes is a non-contact through electrode which is electrically isolated form the chip; at least to radiate heat (Hayasaka: col 11 ln 16).

Re claim 2, Anderson as modified above discloses at least one type of the through electrodes is contact through electrodes electrically connected to that semiconductor chip (Hayasaka, e.g., Figs 8 & 10A-10D; col 13 ln 9, col 14 ln 45).

Re claim 4, Anderson discloses both of the first number and the second number is two or greater (Anderson: Fig 2), so that each of the first (210) and second (220) high-current through electrodes is made up of at least two adjacent ones of the through electrodes which are electrically connected to one another, whereas the signal-routing electrode (205) is made up of only one of the through electrodes.

Re claim 5, Anderson as modified above discloses multiple stacked semiconductor chips (Hayasaka: col 10 ln 46-54), each of the semiconductor chips including a semiconductor device according to claim 1 (Hayasaka: Fig 4).

Re claim 7, Anderson discloses (Fig 2) a chip-stack semiconductor device, comprising:

a plurality of stacked semiconductor chips (Fig 3A, 3C: 310, 340; col 4 ln 35-41), each of the semiconductor chips including a plurality of electrodes (205; col 4 ln 1-2) with equal cross-sectional areas,

wherein at least one of a first high-current electrode (210) connected to a power supply (VDD; col 4 ln 10-12) and a second high-current electrode (220) connected to ground (GND; col 4 ln 4-6) is made up of at least two electrodes which are electrically connected to one another (col 4 ln 3-4), whereas a signal-routing electrode (205) is made up of only one of the electrodes.

Anderson differs from the claimed invention in not disclosing through electrodes and in not disclosing a non-contact through electrode.

Hayasaka discloses (Fig 4) through electrodes (4; col 10 ln 30-34) which electrically link a front surface of the chip to a back surface of the chip.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Anderson in view of Hayasaka by forming at least the peripheral electrodes (205, 212, 220) to be through electrodes which electrically link a

front surface of the chip to a back surface of the chip; at least to allow stacking and connecting more than two chips (Hayasaka: col 10 ln 46-54).

Hayasaka discloses non-contact through electrodes used only for heat radiation (col 11 ln 15-16).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to further modify Anderson in view of Hayasaka such that at least one of the through electrodes is a non-contact through electrode which is not electrically connected to the semiconductor chip; at least to radiate heat (col 11 ln 16).

Re claim 8, Anderson discloses (Fig 2) a chip-stack semiconductor device, comprising multiple stacked semiconductor chips (Fig 3A, 3C: 310, 340; col 4 ln 35-41), each of the semiconductor chips including a number of electrodes (205; col 4 ln 1-2) with equal cross-sectional areas,

wherein a number of adjacent connected ones of the electrodes which are connected to either a ground terminal (220: GND; col 4 ln 4-6) or a power supply terminal (210: VDD; col 4 ln 10-12) of that semiconductor chip (200) is greater than a number (0) of adjacent connected ones of the electrodes (205) which are connected to a particular signal terminal thereof.

Anderson differs from the claimed invention in not disclosing through electrodes and, in not disclosing a non-contact through electrode, and in not expressly disclosing determining the number of the through electrodes.

Hayasaka discloses (Fig 4) through electrodes (4; col 10 ln 30-34) which electrically link a front surface of the chip to a back surface of the chip.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify Anderson in view of Hayasaka by forming at least the peripheral electrodes (205, 212, 220) to be through electrodes which electrically link a front surface of the chip to a back surface of the chip; at least to allow stacking and connecting more than two chips (Hayasaka: col 10 ln 46-54).

Hayasaka discloses non-contact through electrodes used only for heat radiation (col 11 ln 15-16).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to further modify Anderson in view of Hayasaka such that at least one of the through electrodes is a non-contact through electrode which is not electrically connected to the semiconductor chip; at least to radiate heat (col 11 ln 16).

Anderson discloses the electrodes are connected for low impedance (col 4 ln 15-18). It is well known that a larger total conductor cross-section results in lower impedance.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made that the number of the through electrodes be determined in accordance with a magnitude of an electric current to be conducted therethrough; at least to reduce impedance.

Re claims 9, 11, & 12, Anderson as modified by Hayasaka discloses a larger number of adjacent semiconductor chips results in a longer conduction path length (inherent in the structure of Hayasaka Fig 4).

Anderson as modified above differs from the claimed invention only in not expressly disclosing the number of through electrodes used in connecting different numbers of chips.

Anderson discloses the electrodes are connected for low impedance (col 4 ln 15-18). It is well known that a larger total conductor cross-section is used for a longer conduction path length to reduce impedance.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made that a number of those through electrodes which connect n+1 or more adjacent semiconductor chips is greater than a number of those through electrodes which connect n adjacent semiconductor chips, where n is an integer more than or equal to 2; at least to reduce impedance.

Re claims 13, 15, & 16, Anderson as modified by Hayasaka discloses a larger number of adjacent semiconductor chips results in a longer conduction path length (inherent in the structure of Hayasaka Fig 4).

Anderson as modified above differs from the claimed invention only in not expressly disclosing the number of through electrodes is increased with interconnect line length.

Anderson discloses the electrodes are connected for low impedance (col 4 ln 15-18). It is well known that a larger total conductor cross-section is used for a longer conduction path length to reduce impedance.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made that the first and second number of the through electrodes is increased as an interconnect line length through the multiple stacked semiconductor chips is increased; at least to reduce impedance.

Re claims 17, 19, & 20, Anderson as modified by Hayasaka discloses a larger number of adjacent semiconductor chips results in a longer conduction path length (inherent in the structure of Hayasaka Fig 4).

Anderson as modified above differs from the claimed invention only in not expressly disclosing the number of through electrodes is increased in proportion to an interconnect line length.

Anderson discloses the electrodes are connected for low impedance (col 4 ln 15-18). It is well known that a larger total conductor cross-section is used for a proportionally longer conduction path length to reduce impedance.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made that the first and second number of the through electrodes is increased in proportion to an interconnect line length through the multiple stacked semiconductor chips; at least to reduce impedance.

Response to Arguments

Applicant's arguments filed 08/11/2006 have been fully considered but they are not persuasive.

Applicant argues against the references individually ("Anderson and Hayasaka fail to disclose or suggest... non-contact through electrode which is electrically isolated", pg 7 ¶4). One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See MPEP § 2145 (IV).

Applicant alleges features of Hayasaka (pg 8 ¶2) that are not taught in the reference and that do not accurately represent the extent of what the reference would have reasonably suggested to one having ordinary skill in the art. See MPEP § 2123.

Hayasaka discloses "metal plugs only for the purpose of heat radiation" (col 11 ln 15-16) without expressly limiting their implementation. Each plug electrically links the front and back surfaces of the chip it is formed in; and is clearly electrically isolated from the chip portions surrounding the plug (Fig 4: 5; col 10 ln 20-25). Connection can be made to a neighboring chip via the plug (Fig 8: 19), but since "not every chip having the metal plugs need be connected with it's neighbor by means of the plugs" (col 11 ln 13-15), one skilled in the art would reasonably infer that not every plug need be electrically connected to the chip it is formed in. See MPEP § 2144.01.

Applicant has not submitted evidence that one having ordinary skill in the art at the time the invention was made would not have found examiner's proposed combination to be obvious. See MPEP § 2142 (¶1).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew O. Arena whose telephone number is 571-272-5976. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard T. Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Andrew O Arena
23 October 2006

Douglas W. Owens 10/25/06

DOUGLAS W. OWENS
PRIMARY EXAMINER